UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/536,652	05/27/2005	Swain Hong Alfred Yeo	1890-0250	7475

50255 7590 12/14/2007

MAGINOT, MOOR & BECK
111 MONUMENT CIRCLE, SUITE 3000
BANK ONE CENTER/TOWER
INDIANAPOLIS, IN 46204

EXAMINER	
PATEL, REEMA	
ART UNIT	**PAPER NUMBER**
2812	

MAIL DATE	DELIVERY MODE
12/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/536,652	YEO ET AL.	
	Examiner	Art Unit	
	Reema Patel	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 September 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to an amendment filed 9/7/07.

Drawings

1. The drawings were received on 9/7/07. These drawings are acceptable.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 5 and 10-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Uchiyama (U.S. 6,583,834 B1).

4. Regarding claim 5, Uchiyama discloses a method of attaching a flip-chip to a substrate, the flip-chip including a first plurality of electrical contacts with lateral sides and the substrate including a second plurality of electrical contacts with lateral sides, the method comprising:

a. Forming a separate insulating layer of an insulating material (col 6, lines 31-40) on the lateral sides of each of the first plurality of electrical contacts and on the lateral sides of the second plurality of electrical contacts (col 7, lines 50-53; col 8, lines 5-27; Fig. 7);

b. Joining the flip-chip to the substrate using a matrix of insulating material including conductive particles to electrically connect the first plurality of contacts with the second plurality of contacts (col 8, lines 5-27; Fig. 7).

5. Regarding claims 10-11, Uchiyama discloses the matrix of insulating material is an anisotropic conductive adhesive (col 7, lines 50-53).

6. Regarding claim 12, Uchiyama discloses a flip-chip (21, Fig. 7) having a first surface including a first plurality of electrical contacts (22, Fig. 7), the first plurality of electrical contacts including lateral sides; a first electrically insulating film (5, Fig. 7) formed on the lateral sides of the first plurality of electrical contacts; a substrate (11, Fig. 7) having a second surface including a second plurality of electrical contacts (12, Fig. 7), the second plurality of electrical contacts including lateral sides, and the second plurality of electrical contacts facing the first plurality of electrical contacts; a second separate electrically insulating film (4, Fig. 7) formed on the lateral sides of the second plurality of electrical contacts; and a matrix of insulating material (1, Fig. 7) including electrically conductive particles (3, Fig. 7) between the flip chip and the substrate (col 7, lines 50-53; col 8, lines 5-23).

7. Regarding claims 13-14, Uchiyama discloses the matrix of insulating material is an anisotropic conductive adhesive (col 7, lines 50-53).

8. Regarding claims 15-16, Uchiyama discloses the substrate is an integrated circuit and the electrical contacts comprise gold bumps (col 8, lines 5-15).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchiyama (U.S. 6,583,834 B1) as applied to claim 5 above, and further in view of Jimarez et al. (U.S. 2001/0018230 A1; hereinafter 'Jimarez').

11. Regarding claim 6, Uchiyama discloses forming separate insulating layers on the lateral sides of a plurality of contacts of both a flip chip and substrate (see claim 5 rejection). Yet, Uchiyama does not disclose the method of forming the insulating layer. However, Jimarez discloses a method of forming an insulating layer on the sidewall of a conductive contact. Jimarez discloses forming a coating, curing, and removing portions overlying the contacts by polishing ([0059]). The advantage of this method is the ability to remove portions of the insulating layer formed on the contacts easier. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Uchiyama with forming the separate insulating layers on the lateral sides of the contacts of a flip chip and substrate, with the method of Jimarez, so as to remove portions of the insulating layer formed on the contacts with ease.

12. Regarding claims 7-8, Jimarez discloses grinding the portions of the insulating layer overlying the contacts ([0059]) but does not disclose specifically chemical

mechanical polishing (CMP) or backlapping. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to polish with CMP or a backlapping tool since the examiner takes Official Notice of the equivalence of grinding, CMP, and backlapping for their use in the semiconductor art and the selection of any of these known equivalents to etch the surface of a layer flat would be within the level of ordinary skill in the art.

13. Regarding claim 9, Jimarez discloses using a photosensitive resin as the insulating layer ([0059]).

14. Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchiyama (U.S. 6,583,834 B1) in view of Jimarez et al. (U.S. 2001/0018230 A1; hereinafter 'Jimarez').

15. Regarding, claim 17, Uchiyama discloses the following:

- Forming an insulating layer (col 6, lines 31-40) on the lateral sides of each of the first plurality of electrical contacts and on the lateral sides of the second plurality of electrical contacts (col 7, lines 50-53; col 8, lines 5-27; Fig. 7);
- Joining the flip-chip to the substrate using a matrix of insulating material including conductive particles to electrically connect the first plurality of contacts with the second plurality of contacts (col 8, lines 5-27; Fig. 7).

16. Yet, Uchiyama does not disclose the method of forming the insulating material formed on the lateral sides of the contacts of the flip chip and substrate. However, Jimarez discloses a method of forming a photosensitive insulating layer on the sidewall

of a conductive contact. Jimarez discloses forming a coating, curing, and removing portions overlying the contacts by polishing ([0059]). The advantage of this method is the ability to remove portions of the insulating layer formed on the contacts easier.

Furthermore, Jimarez does not disclose that the polishing occurs by CMP. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to polish with CMP since the examiner takes Official Notice of the equivalence of grinding and CMP for their use in the semiconductor art and the selection of any of these known equivalents to etch the surface of a layer to a flat level would be within the level of ordinary skill in the art.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Uchiyama with forming the separate insulating layers on the lateral sides of the contacts of a flip chip and substrate, with the method of Jimarez, so as to remove portions of the insulating layer formed on the contacts with ease.

17. Regarding claims 18-19, Uchiyama discloses the matrix of insulating material is an anisotropic conductive adhesive (col 7, lines 50-53).

Response to Arguments

18. Applicant's arguments with respect to claims 5-19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reema Patel whose telephone number is 571-270-1436. The examiner can normally be reached on M-F, 8:00-4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RSP

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER